

Client's ref.: TSMC2003-1244

Our ref.: 0503-A30213us/final/spin(王珠鄰)/Nelson

What Is Claimed Is:

1 1. A method of forming dielectric layers with various
2 thicknesses on a substrate, comprising the steps of:
3 providing a first device region and a second device region
4 on the substrate;
5 growing a first oxide layer on the substrate ;
6 depositing a dielectric layer with a first thickness on the
7 first oxide layer;
8 removing the dielectric layer and the underlying first
9 oxide layer on the second device region to expose the
10 substrate; and
11 growing a second oxide layer with a second thickness less
12 than the first thickness on the substrate of the
13 second device region.

1 2. The method of claim 1, wherein the substrate further
2 comprises a third device region.

1 3. The method of claim 2, wherein the third device region
2 is a core device region for low voltage operation.

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1 4. The method of claim 2, further comprising the steps
2 of:

3 removing the dielectric layer and the underlying first
4 oxide layer on the third device region to expose the
5 substrate; and

6 growing a third oxide layer with a third thickness less than
7 the first thickness on the substrate of the third
8 device region and on the second oxide layer.

1 5. The method of claim 4, wherein third oxide layer is
2 grown by thermal oxidation.

1 6. The method of claim 4, wherein the third thickness is
2 about 30 to 60Å.

1 7. The method of claim 1, wherein the first device region
2 is a power device region for high voltage operation.

1 8. The method of claim 1, wherein the second device
2 region is an I/O device region for low voltage operation.

1 9. The method of claim 1, wherein the first oxide layer
2 is grown by thermal oxidation.

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1 10. The method of claim 1, wherein the dielectric layer
2 is a high temperature oxide layer formed by CVD.

1 11. The method of claim 1, wherein the first thickness is
2 about 300 to 3000Å.

1 12. The method of claim 1, wherein second oxide layer is
2 grown by thermal oxidation.

1 13. The method of claim 1, wherein the second thickness
2 is about 40 to 70Å.

1 14. A method of forming gate dielectric layers with
2 various thicknesses on a substrate, comprising the steps of:
3 providing a first active region and a second active region
4 on the substrate;
5 forming a first thermal oxide layer on the substrate;
6 depositing a blanket dielectric layer with a first
7 thickness overlying the substrate;
8 forming a first masking layer overlying the substrate
9 except over the second active region;

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10 etching the dielectric layer and the underlying first
11 thermal oxide layer on the second active region using
12 the first masking layer as an etch mask to expose the
13 substrate;
14 removing the first masking layer;
15 forming a second thermal oxide layer with a second
16 thickness less than the first thickness on the second
17 active region; and
18 forming a first gate on the dielectric layer on the first
19 active region and a second gate on the second thermal
20 oxide layer on the second active region.

1 15. The method of claim 14, wherein the substrate further
2 comprises a third active region.

1 16. The method of claim 15, wherein the third active
2 region is separated from the second active region by a shallow
3 trench isolation region.

1 17. The method of claim 15, wherein before forming the
2 first and second gates, further comprising the steps of:

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3 forming a second masking layer overlying the substrate
4 except over the third active region;
5 removing the dielectric layer and the underlying first
6 thermal oxide layer on the third active region to
7 expose the substrate;
8 removing the second masking layer; and
9 forming a third thermal oxide layer with a third thickness
10 less than the first thickness on the third active
11 region and on the second thermal oxide layer.

1 18. The method of claim 17, wherein the second masking
2 layer is a photoresist layer.

1 19. The method of claim 17, wherein the step of forming
2 the first and second gates further comprises forming a third gate
3 on the third thermal oxide layer on the third active region.

1 20. The method of claim 17, wherein the third thickness
2 is about 30 to 60Å.

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1 21. The method of claim 14, wherein the first active
2 region and the second active region are separated by a shallow
3 trench isolation region.

1 22. The method of claim 14, wherein the dielectric layer
2 is a high temperature oxide layer formed by CVD.

1 23. The method of claim 14, wherein the first thickness
2 is about 300 to 3000Å.

1 24. The method of claim 14, wherein the first masking
2 layer is a photoresist layer.

1 25. The method of claim 14, wherein the second thickness
2 is about 40 to 70Å.

1 26. A method of forming an integrated circuit having gate
2 oxide layers with multiple thicknesses, comprising the steps of:
3 providing a substrate having a first active region, a
4 second active region, and a third active region;
5 performing a first oxidation to form a first oxide layer
6 on the substrate;

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7 depositing a blanket high temperature oxide layer with a
8 first thickness overlying the substrate;
9 forming a first photoresist layer on the high temperature
10 oxide layer except over the second active region;
11 etching the high temperature oxide layer and the underlying
12 first oxide layer on the second active region using
13 the first photoresist layer as an etch mask to expose
14 the substrate;
15 removing the first photoresist layer;
16 performing a second oxidation to form a second oxide layer
17 with a second thickness less than the first thickness
18 on the second active region;
19 forming a second photoresist layer overlying the
20 substrate except over the third active region;
21 removing the high temperature oxide layer and the
22 underlying first oxide layer on the third active
23 region to expose the substrate;
24 removing the second photoresist layer;
25 performing a third oxidation to form a third oxide layer
26 with a third thickness less than the first thickness

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27 on the third active region and on the second oxide
28 layer on the second active region; and
29 forming a first gate on the high temperature oxide layer
30 on the first active region, a second gate on the
31 second oxide layer on the second active region, and
32 a third gate on the third thermal oxide layer on the
33 third active region.

1 27. The method of claim 26, wherein the first, second, and
2 third active regions are separated by a shallow trench isolation
3 region.

1 28. The method of claim 26, wherein the first thickness
2 is about 300 to 3000Å.

1 29. The method of claim 26, wherein the second thickness
2 is about 40 to 70Å.

1 30. The method of claim 26, wherein the third thickness
2 is about 30 to 60Å.

1 31. The method of claim 26, wherein the high temperature
2 oxide layer is formed by CVD.